

Kolloquiumsvortrag

Donnerstag, 26.05.2011, 16 Uhr c.t., F384

The Quest for the Limits of Automatic Program Verification

*Dr. Antti Siirtola,
Oulu University, Finland*

Due to increasing amount of parallelism, concurrency and distribution, systems have become difficult to design and analyse. In this effort, formal verification, which can be thought as exhaustive testing, has turned out to be useful. Unfortunately, many verification methods require a lot of user intervention or only apply to systems which are representable in a finite, algorithmically manageable form. These are major problems because manual reasoning is prone to errors and the state space of many systems, especially software applications, is unbounded.

On the other hand, in practice, the resources are always limited. That is why a running application can never reach infinitely many states. A typical approach is to model a system and a specification parameterised by the restrictions of the execution environment. When the model is instantiated for all the values the parameters are allowed to take, an (infinite) family of finite-state systems and specifications is obtained. The question whether all the instances are correct is known as the parameterised verification problem (PVP).

As all software systems can be considered multi-parameterised finite-state machines where the parameters determine the (maximum) number of replicated components (like objects), their relationships (a system topology), the size of basic data types and the structure of data, the parameterised verification is of high practical relevance. On the other hand, because PVP is undecidable in general, automating parameterised verification is theoretically challenging.

In this talk, we explore the limits of automatic program verification; we review the history of algorithmic parameterised verification and give an insight to the latest developments in the field.